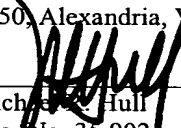


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ju-Il Lee)	I hereby certify that this paper and the
)	documents referred to as enclosed
Serial No.: To be Assigned)	therewith are being deposited with the
)	United States Postal Service as first class
Filed: September 24, 2003)	mail, postage prepaid, on September 24,
)	2003 , in an envelope addressed to
For: Method for Manufacturing CMOS)	Commissioner for Patents, P.O. Box
Image Sensor Using Spacer Etching)	1450, Alexandria, Virginia 22313-1450.
Barrier Film)	
)	
Group Art Unit: To be Assigned)	Michael R. Hull
)	Reg. No. 35,902
Examiner: To be Assigned)	Attorney for Applicant

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Submitted herewith for consideration by the examiner are copies of the documents identified on the attached PTO-1449. Entry and consideration of the submitted documents is solicited.

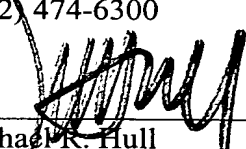
The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855. A copy of this paper is enclosed.

Respectfully submitted,

MARSHALL, GERSTEIN & BORUN LLP
6300 Sears Tower
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September 24, 2003

By:


Michael R. Hull
Reg. No. 35,902

Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. 29926/39504	Serial No. To be Assigned
INFORMATION DISCLOSURE STATEMENT		Applicant Ju-Il Lee	
		Filing Date 09/25/03	Group To be Assigned

U.S. PATENT DOCUMENTS							
*Examiner Initials		Document Number	Issue Date	Name	Class	Subclass	Filing Date if Appropriate

FOREIGN PATENT DOCUMENTS								
*Examiner Initials		Document Number	Publication Date	Country	Class	Subclass	Translation	
							Yes	No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)		
		Furumiya et al., <i>High-Sensitivity and No-Crosstalk Pixel Technology for Embedded CMOS Image Sensor</i> , IEEE Transactions on Electron Devices, Vol. 48, No. 10, October 2001, Pages 2221-2227.
		Nallapati et al., <i>Influence of Plasma Induced Damage During Active Etch on Silicon Defect Generation</i> , 2000 5 th International Symposium on Plasma Process-Induced Damage, May 23-24, Santa Clara, CA, USA, 2000 American Vacuum Society, Pages 61-64.

EXAMINER	DATE CONSIDERED
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance <u>and</u> not considered. Include copy of this form with next communication to applicant.</p>	